

# CPAD 2021

Virtual Event @ Stony Brook University, March 18-22, 2021



## Time measurements using Ultra-Fast Silicon Detectors with a 120 GeV proton beam for the TOPSiDE concept at the Electron-Ion Collider

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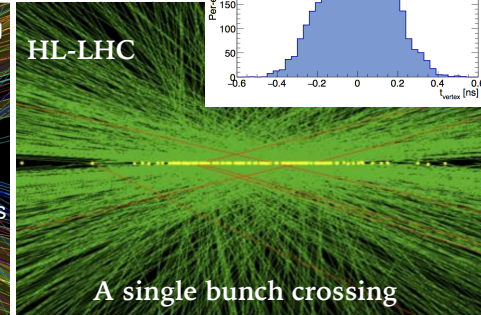
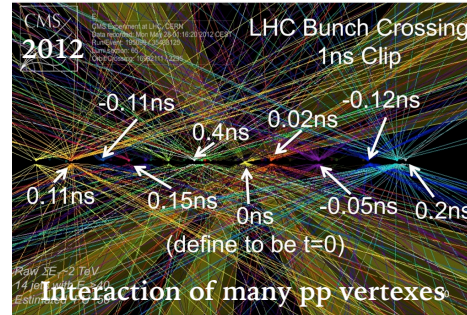
18 - 22 March 2021  
Stony Brook, NY

# Outline

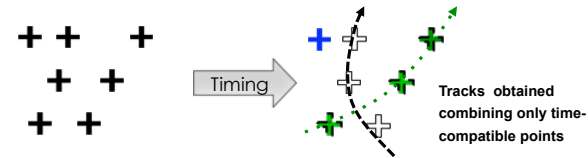
- Introduction to UFSDs
  - Motivation for Ultra-Fast Silicon Detectors (UFSD)
  - UFSD for TOPSiDE at the Electron-Ion Collider
  - Timing Measurements
- LGAD Test Setup
  - LGAD Measurement Setup
  - Testing of LGADs at the Fermilab Test Beam
- Results and Summary
- Outlook

# Motivation for UFSDs

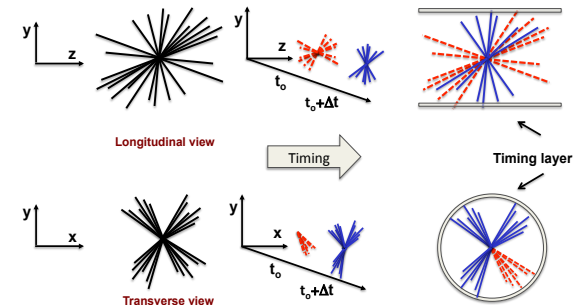
- ❖ One bunch crossing with  $\sim 50$  overlapping events recorded by the CMS experiment in 2012
- ❖ The situation will substantially change at HL-LHC - the order of 150–200 events per bunch crossing
- ❖ The time-dimension improves the reconstruction process by considering only time-compatible hits
- ❖ Discarding those hits that cannot be associated to a track.
- ❖ Particle Identification using **Time-Of-Flight method**



(1)

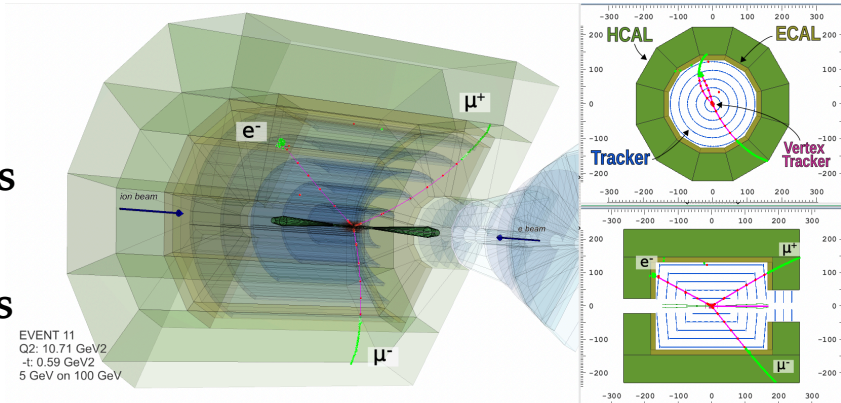
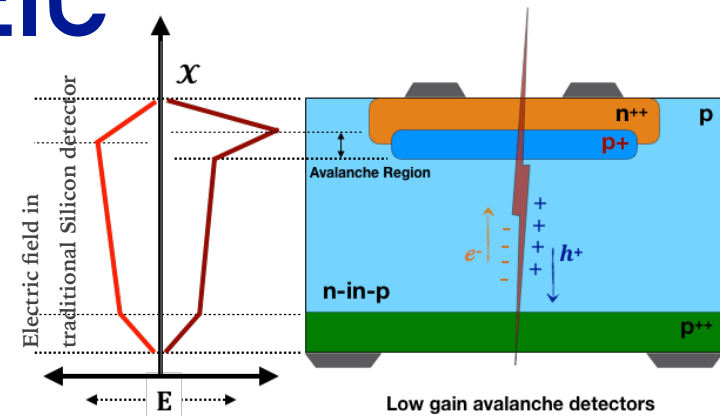


(2)



# UFSD for TOPSiDE at EIC

- ❖ Low-Gain Avalanche Diode (LGAD)
  - ❖ Internal gain layer ( $n^{++}$ -  $p^+$  -  $p$  -  $p^{++}$ )
- ❖ High E-field in gain region
  - ❖ Multiplication process
  - ❖ Provides gain of 10-70 w/o breakdown
- ❖ Electron-Ion Collider: Polarized ep, eA collider
  - ❖ Centre of mass energies up to  $\sim 140$  GeV
  - ❖ Luminosity  $\sim 10^{33}$ - $10^{34}$   $\text{cm}^{-2}\text{s}^{-1}$
- ❖ Measurement and identification of particles
  - ❖ Silicon tracker + Calorimeter - 5D info
- ❖ Silicon sensor with time resolution  $\sim 10$  ps
  - ❖ kaon-pion separation up to  $7 \text{ GeV}/c$



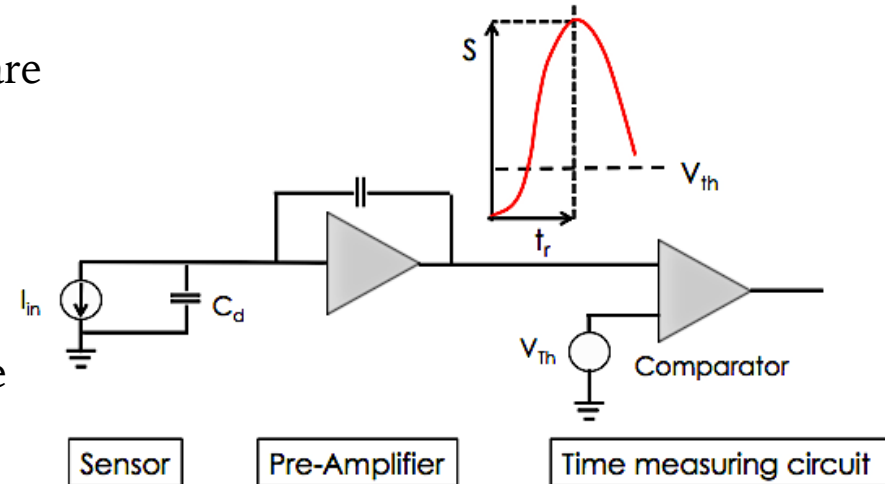


# Timing Measurements

Time resolution of the Silicon detector can be expressed as contribution of,

$$\sigma_t^2 = \sigma_{TimeWalk}^2 + \sigma_{Jitter}^2 + \sigma_{LandauNoise}^2 + \sigma_{Distortion}^2 + \sigma_{TDC}^2$$

- ❖ **Timing capabilities** of the silicon detector are characterized by signal at preamplifier output and TDC binning
- ❖ **Time of arrival** is set when signal crosses the comparator threshold
- ❖ **Timing resolution** is measured as RMS of the timing difference (or TOF of a MIP) between the device-under-test (DUT) and the trigger.



A simple time-tagging detector

# Timing Measurements

- ❖ **Time Walk:** the voltage value  $V_{th}$  is reached at different times by signals of different amplitude

$$\sigma_{TimeWalk} = \left[ \frac{V_{th}}{dv/dt} \right]_{RMS}$$

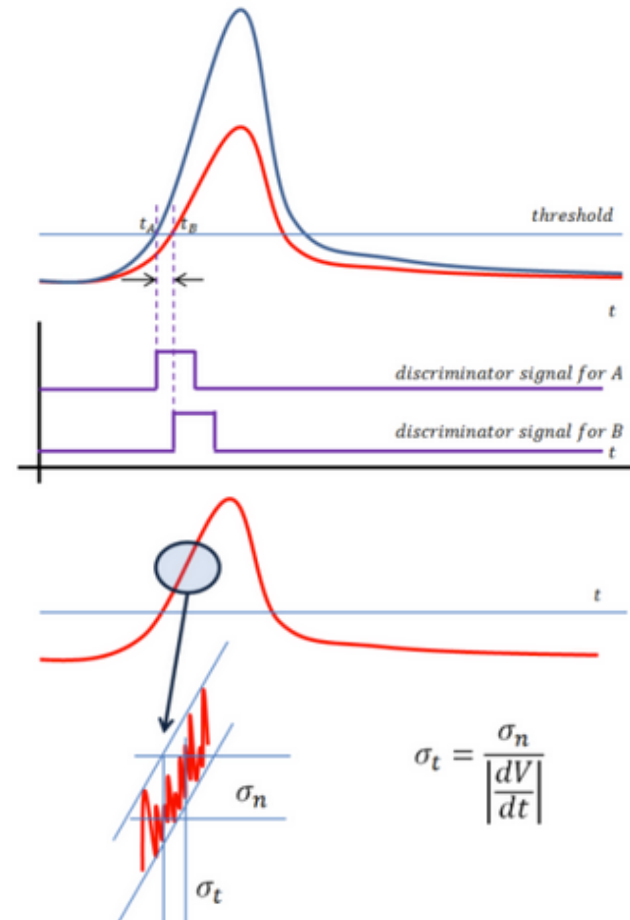
Constant fraction discriminator (CFD) with TOA defined at % of signal amplitude reduces time-walk contribution

- ❖ **Jitter:** variation in time caused by the noise in the system

$$\sigma_{Jitter} = \frac{Noise}{dV/dt}$$

The noise is summed to the signal, causing amplitude variations

The predominant contribution to the timing resolution

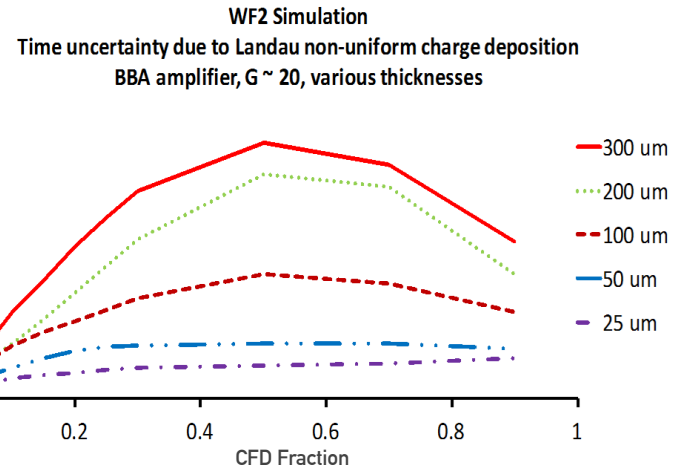


# Timing Measurements

- ❖ **Landau Noise:** introduced by a particle's non-uniform charge deposition along its passage  
Decreases with thickness of the sensor  
Jitter and Landau noise contribute almost equally
- ❖ **Distortion:** The signal distortion is negligible in silicon for the saturated drift velocity and uniform weighting field.
- ❖ **TDC:** The TDC effect is minimal in most of the cases

$$\sigma_{TDC} = \frac{TDC_{bin}}{\sqrt{12}}$$

The time resolution is minimized by maximizing the slew rate  $dV/dt$  of the signal and minimizing the noise

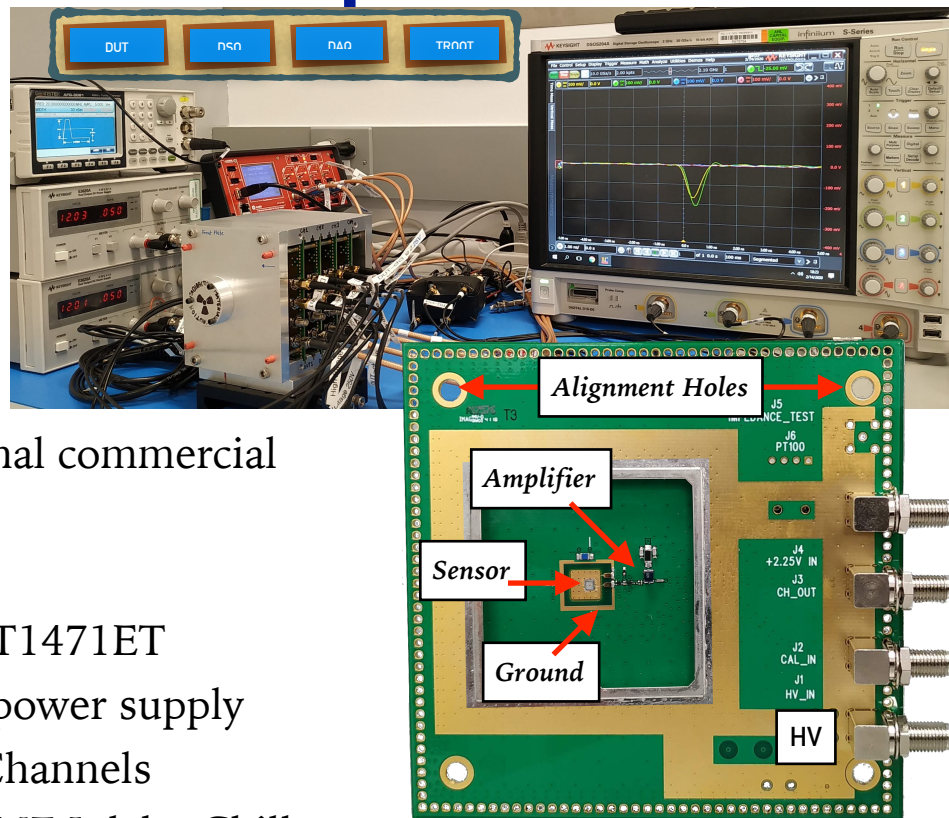


Thinner Sensor => faster rise time => larger slew rate

We need large and short signals!

# LGAD Measurement Setup

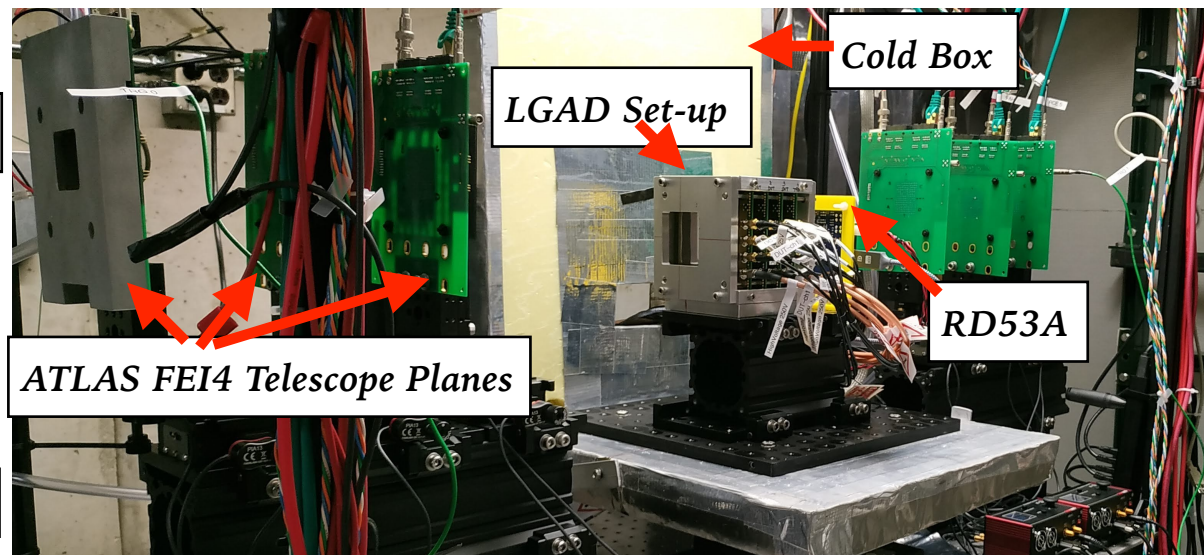
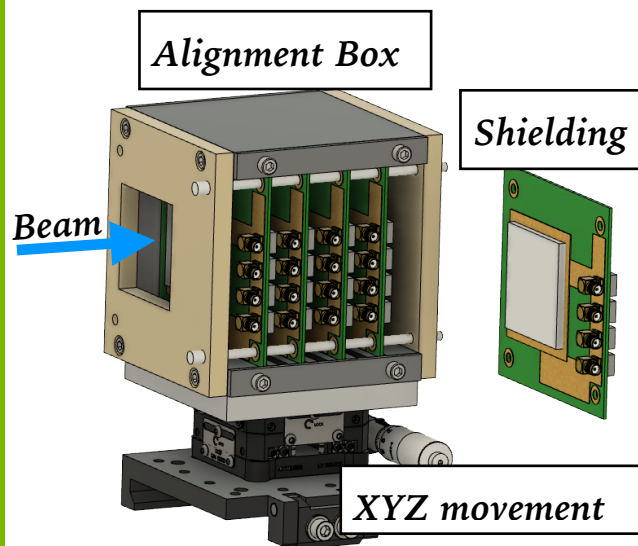
- ❖  $\beta$ -Telescope
    - ❖ Lab bench setup with  $\text{Sr}^{90}$  source
  - ❖ Single channel readout board
    - ❖  $10 \times 10 \text{ cm}^2$ ; impedance of  $50\Omega$
    - ❖ Wide bandwidth 2 GHz and gain 10
    - ❖ Total trans-impedance of  $4700\Omega$
    - ❖ The amplifier is followed by an external commercial amplifier with gain 10
  - ❖ Signal acquisition
    - ❖ High Voltage Power Supply CAEN DT1471ET
    - ❖ KEYSIGHT E3620A DC low voltage power supply
    - ❖ KEYSIGHT DSOS204A infiniium 4-Channels
- Measurements at  $-30^\circ\text{C}$  using FP89-ME Julabo Chiller





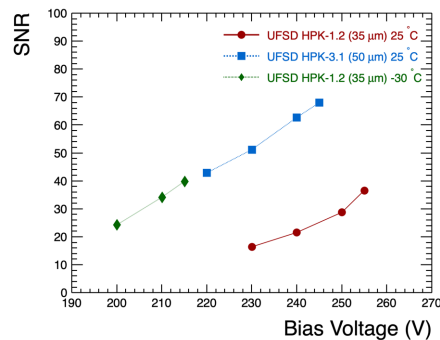
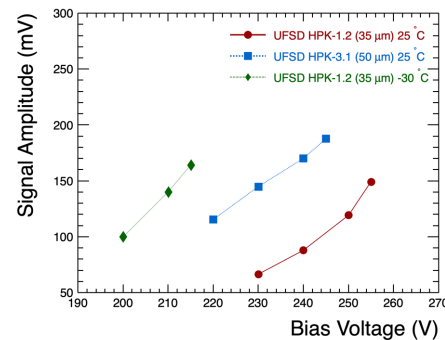
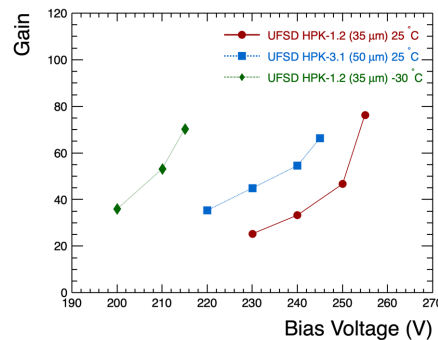
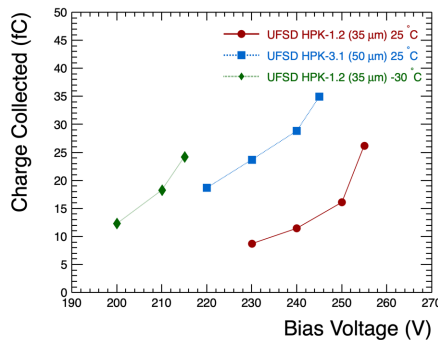
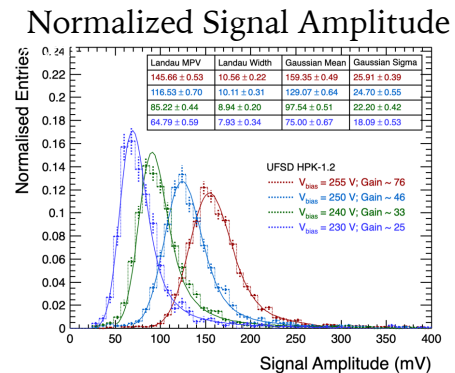
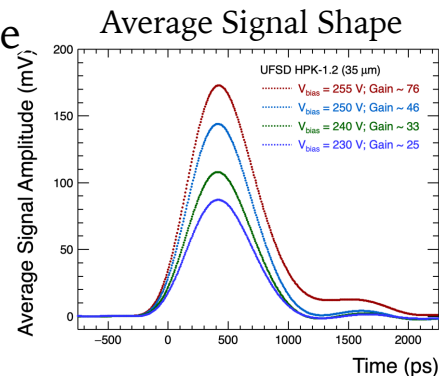
# Fermilab Test Beam Set-up

- ❖ Proton Beam with momentum 120 GeV
- ❖ Sensors HPK 1.2 (35 $\mu$ m), 3.1 (50 $\mu$ m) were tested
- ❖ In collaboration with UCSC and BNL groups



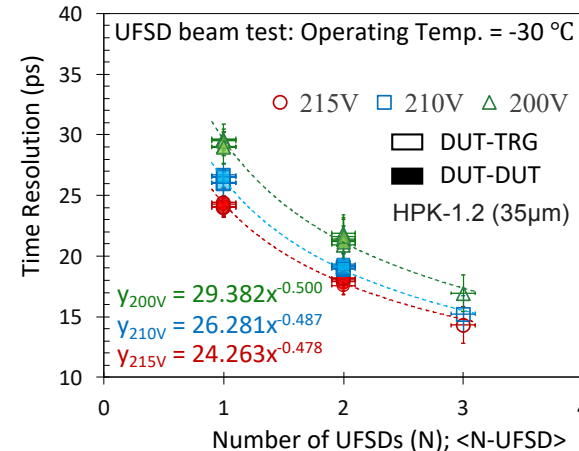
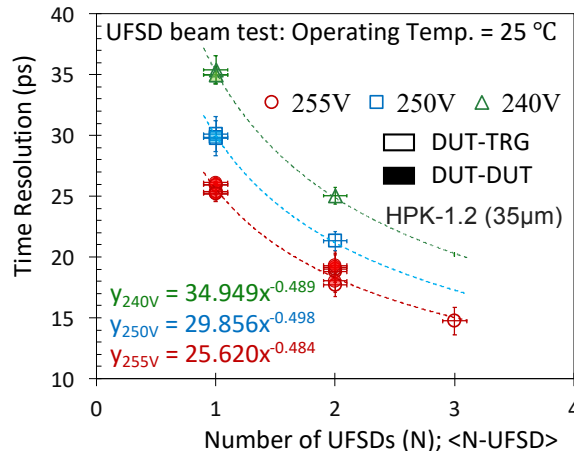
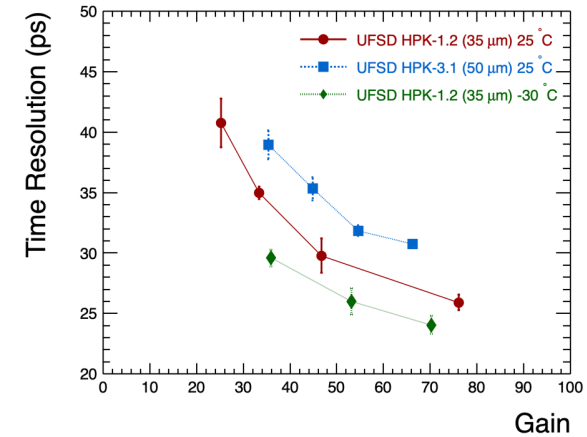
# Results and Summary

- Normalized signal amplitude vs. Bias Voltage
- Charge Multiplication increases with bias voltage increasing the Gain
- Signal Amplitude, Signal to Noise Ratio, Jitter, Rise Time as function of voltage bias and temperature



# Results and Summary

- ❖ Timing resolution for 3 layers of LGADs
- ❖ Timing resolution improves at low temperature but restricted by the lower breakdown voltage
- ❖ Very short rise time of  $\sim 350$ -400 ps were obtained
- ❖ Achieved timing resolution of  $14.31 \pm 1.52$  ps
- ❖ M. Jadhav et al., arXiv:2010.02499; Accepted at JINST



# Outlook

## Argonne Micro-Assembly Facility - clean room

- ❖ Probe Station
- ❖ Thermal Chamber
- ❖ Wire-Bonders
- ❖ SmartScope ZIP for Metrology
- ❖ 3D printer
- ❖ ATLAS telescope and LGAD setup



## Ongoing Development

- ❖ Designing a telescope structure for multichannel readout system
- ❖ Upgrading DAQ from software based CFD to digitizer based: Beyond DSO trigger
- ❖ R&D of LGAD sensors and modules
  - ✓ Goal is to reach 10 ps of timing resolution
  - ✓ Testing CFD read-out boards designed at Argonne
  - ✓ Monolithic LGAD simulations and designing
- ❖ Analysis of data collected at Fermilab test beam facility with 120 GeV proton for different AC-LGADs with multi-channel read-out boards.
- ❖ Argonne is part of LGAD consortium for EIC

Thank You!